Amendments to the Claims:

Please add new dependent claims 99-104 and amend claims 1, 92, and 98 as shown below. This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1.(Presently Amended) A method of simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a plurality of circuit stress time values;

supplying aging model information on selected ones of the components;

simulating the behavior of the fresh circuit to determine for each of the selected components a component degradation parameter relative to circuit stress time; and

determining the degraded operation of the circuit by simulating in a single run the operation of the circuit with the specified components using their respective aging model information and respective relative component degradation parameter at the plurality of supplied circuit stress time values.

2.(Original) The method of claim 1, wherein said degradation of the circuit is due to hot-carrier effects.

3.(Original) The method of claim 1, wherein the simulating is performed using a SPICE type circuit simulator.

4.(Original) The method of claim 1, wherein the simulating is performed using a timing simulation type circuit simulator.

5.(Original) The method of claim 1, wherein the aging model information on the selected ones of the components is derived from electrical test data.

6.(Original) The method of claim 1, wherein said simulating the behavior of the fresh circuit determines the waveforms at the nodes to which the selected ones of the components are connected relative to an input waveform.

7.(Original) The method of claim 1, wherein determining the degraded operation of the circuit comprises determining the circuit's speed at the supplied circuit age parameters.

8. (Cancelled)

9.(Previously Presented) The method of claim 93, wherein the distinct sets of components each form different functional blocks.

10.(Previously Presented) The method of claim 93, wherein a first of said sets of components is an analog block and a second of said sets of components is a digital block.

11.(Original) The method of claim 10, wherein the performance criterion of the first set is transconductance and the performance criterion of the second set is drain to source current.

12.(Previously Presented) The method of claim 93, wherein the distinct sets of components consist of different device types.

13.(Original) The method of claim 12, wherein a first of said different device types is an NMOS and a second of said different device types is a PMOS.

14.(Original) The method of claim 13, wherein the PMOS performance criterion is leakage current.

15.(Original) The method of claim 13, wherein the NMOS performance criterion is driving capability.

16.(Original) The method of claim 12, wherein a first of said different device types is a MOSFET and a second of said different device types is a bipolar junction transistor.

17.(Original) The method of claim 16, wherein the bipolar junction transistor performance criterion is leakage current.

18.(Previously Presented) The method of claim 93, wherein the distinct sets of components employ different models for simulating the same device type.

19.(Previously Presented) The method of claim 93, wherein the distinct sets of components consist of the same device type.

20.(Previously Presented) The method of claim 93, wherein the distinct sets of components form functional blocks performing the same function.

21. (Cancelled)

22.(Previously Presented) The method of claim 94, wherein the first and second sets of components each form different functional blocks.

23.(Previously Presented) The method of claim 94, wherein the second set of components form a digital block.

24.(Original) The method of claim 23, wherein the specified degradation level is expressed in terms of drain to source current degradation.

25.(Previously Presented) The method of claim 94, wherein the second set of components is an analog block.

26.(Original) The method of claim 25, wherein the specified degradation level is expressed in terms transconductance degradation

27.(Previously Presented) The method of claim 94, wherein the first and second sets of components each consist of different device types.

28.(Original) The method of claim 27, wherein the second set of components consists of PMOS transistors.

29.(Original) The method of claim 28, wherein the specified degradation level is expressed in terms of leakage current degradation.

30.(Original) The method of claim 27, wherein the second set of components consists of NMOS transistors.

31.(Original) The method of claim 30, wherein the specified degradation level is expressed in terms of driving capability degradation.

32.(Original) The method of claim 27, wherein the second set of components consists of bipolar junction transistors.

33.(Original) The method of claim 32, wherein the specified degradation level is expressed in terms of leakage current degradation.

34.(Previously Presented) The method of claim 94, wherein the first and second sets of components employ different models for simulating the same device type.

35.(Previously Presented) The method of claim 94, wherein the first and second sets of components each consist of the same device type.

36.(Previously Presented) The method of claim 94, wherein the first and second sets of components form functional blocks performing the same function.

37.(Previously Presented) The method of claim 94, wherein the degradation level of the second set of selected components is specified as a relative component degradation parameter with respect to the component degradation parameter of the first set of components.

38.(Previously Presented) The method of claim 94, wherein the degradation level of the second set of selected components is expressed in terms of age.

39.(Previously Presented) The method of claim 94, wherein the degradation level of the second set of selected components is expressed in terms of lifetime.

40-51. (Cancelled)

52.(Previously Presented) The method of claim 95, wherein the selected components are MOSFETs.

53.(Original) The method of claim 52, wherein said degradation of the circuit is due to hot carrier effects.

54.(Original) The method of claim 52, wherein for each of said selected components more than one of said plurality of independent current sources are connected between the source and drain terminals of the non-aged version.

55.(Original) The method of claim 52, wherein said method further includes:

determining the magnitude of the respective current in each of the independent current sources, said determining comprising:

supplying a physical model of the current magnitude; and

establishing the values of the coefficients in the physical model from electrical test data.

56.(Original) The method of claim 52, wherein the degradation level of the selected components is expressed in terms of lifetime.

57.(Original) The method of claim 52, wherein the degradation level of the selected components is expressed in terms of age.

58.(Previously Presented) The method of claim 95, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said revising the netlist is embedded in the circuit simulator.

59. (Cancelled)

60. (Cancelled)

61.(Previously Presented) The method of claim 97, wherein the selected components are MOSFETs and said incorporating the aging of the selected components comprises including the time dependence of the drain to source current.

62.(Original) The method of claim 61, wherein said incorporating the aging of the selected components comprises including the time dependence of the substrate current.

63.(Original) The method of claim 61, wherein said incorporating the aging of the selected components comprises including the time dependence of the gate current.

64.(Previously Presented) The method of claim 97, wherein said simulating the behavior of the circuit to determine for each of the selected components a component degradation parameter relative to circuit age comprises:

simulating the behavior of the fresh circuit to determine for each of the selected components an intermediate component degradation parameter relative to circuit stress time;

determining the degraded operation of the circuit at an intermediate circuit stress time value by simulating the operation of the circuit with the each of the specified components using the respective aging model information and respective relative intermediate component degradation parameter at the intermediate circuit stress time value; and

simulating the behavior of the degraded circuit at the intermediate circuit stress time value to determine for each of the selected components a component degradation parameter relative to circuit age, wherein the intermediate circuit stress time value is less than one of the circuit stress time values.

65.(Previously Presented) The method of claim 97, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said incorporating the aging of the selected components by updating the models of said circuit simulator is embedded in the circuit simulator.

66-75. (Cancelled)

76.(Previously Presented) The method of claim 98, wherein said determining comprises:

revising the netlist, wherein each of said selected components is replaced by a non-aged version of the selected component and a plurality of independent current sources corresponding to different mechanisms with distinct quantized relative degradation level connected between the terminals of the non-aged version, the magnitude of the respective quantized current in each of the current sources determined from the aging model information of component; and

determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist, the independent current magnitudes derived form the

respective aging model information and respective relative degradation level at the supplied circuit stress time value.

77.(Previously Presented) The method of claim 98, wherein said simulating the operation of the circuit is performed with a circuit simulator and wherein said quantizing is embedded in the circuit simulator.

78-90. (Cancelled)

91.(Previously Presented) A computer readable storage device embodying a program of instructions executable by a computer to perform the method of any one of claims 1, and 93-98.

92.(Presently Amended) A method for transmitting a program of instructions executable by a computer to perform a process of simulating the degradation of a circuit, said method comprising:

causing the transmission to a client device a program of instructions, thereby enabling the client device to perform, by means of such program, the process of ~~the method of any one of claims 1, and 93-98~~ simulating the degradation of a circuit, comprising:

providing a netlist specifying the components of the circuit;

supplying a plurality of circuit stress time values;

supplying aging model information on selected ones of the components;

simulating the behavior of the fresh circuit to determine for each of the selected components a component degradation parameter relative to circuit stress time; and

determining the degraded operation of the circuit by simulating in a single run the operation of the circuit with the specified components using their respective aging model information and respective relative component degradation parameter at the plurality of supplied circuit stress time values.

93.(Previously Presented) The method of claim 1, wherein the circuit includes a plurality of distinct sets of components, the method further comprising:

supplying an independent performance criterion for each set of said plurality of distinct sets of components, and

wherein said supplying aging model information includes supplying aging model information on selected components from each of said sets of components,

wherein each of the selected components' relative degradation parameter is determined using the respective performance criteria of the set to which the selected component belongs,

and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with each of the specified components using the respective aging model information and respective relative component degradation parameter at the supplied circuit stress time values.

94.(Previously Presented) The method of claim 1, wherein said supplying aging model information includes supplying aging model information on a first set of selected components of the circuit and wherein said simulating the behavior of the fresh circuit includes simulating the behavior of the fresh circuit to determine for each of the first selected set of components a component degradation parameter relative to circuit stress time, the method further comprising:

specifying the degradation level of a second set of selected components of the circuit, wherein the elements of the first set and the second set of components are distinct,

and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with each of the first set of specified components using the respective aging model information and respective relative component degradation parameter at the supplied circuit stress time values and with each of the second set of specified components using the respective specified degradation level.

95.(Previously Presented) The method of claim 1, further comprising:

revising the netlist, wherein each of said selected components is replaced by a non-aged version of the selected component and a plurality of independent current sources corresponding to different mechanisms connected between the terminals of the non-aged version, wherein the magnitude of the current relative to a circuit stress time in each of the current sources of a component is determined from the aging model information of the component and a distinct mechanism degradation parameter derived from the component degradation parameter; and

wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist at the supplied circuit stress time values.

96.(Previously Presented) The method of claim 95, wherein said simulating the behavior is performed using a circuit simulator and includes incorporating the aging of the selected components by updating the models of said circuit simulator.

97.(Previously Presented) The method of claim 1, wherein said simulating the behavior is performed using a circuit simulator and includes incorporating the aging of the selected components by updating the models of said circuit simulator,

and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit at the supplied stress time values by simulating the operation of the circuit with the each of the specified components using the respective aging model information and respective relative component degradation parameter at the supplied stress time values.

98.(Presently Amended) The method of claim 1, wherein said degradation parameter is a degradation level relative to circuit stress time, the method further comprising:

quantizing each of said relative degradation levels to one of a plurality of discrete values, and

wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with

the specified components using their respective aging model information and respective quantized relative degradation level at the supplied circuit stress time ~~value~~ values.

99.(New) The method of claim 92, wherein the circuit includes a plurality of distinct sets of components, the process further comprising:

supplying an independent performance criterion for each set of said plurality of distinct sets of components, and

wherein said supplying aging model information includes supplying aging model information on selected components from each of said sets of components,

wherein each of the selected components' relative degradation parameter is determined using the respective performance criteria of the set to which the selected component belongs,

and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with each of the specified components using the respective aging model information and respective relative component degradation parameter at the supplied circuit stress time values.

100.(New) The method of claim 92, wherein said supplying aging model information includes supplying aging model information on a first set of selected components of the circuit and wherein said simulating the behavior of the fresh circuit includes simulating the behavior of the fresh circuit to determine for each of the first selected set of components a component degradation parameter relative to circuit stress time, the process further comprising:

specifying the degradation level of a second set of selected components of the circuit, wherein the elements of the first set and the second set of components are distinct,

and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with each of the first set of specified components using the respective aging model information and respective relative component degradation parameter at the supplied circuit stress time values and with each of the second set of specified components using the respective specified degradation level.

101.(New) The method of claim 92, the process further comprising:

revising the netlist, wherein each of said selected components is replaced by a non-aged version of the selected component and a plurality of independent current sources corresponding to different mechanisms connected between the terminals of the non-aged version, wherein the magnitude of the current relative to a circuit stress time in each of the current sources of a component is determined from the aging model information of the component and a distinct mechanism degradation parameter derived from the component degradation parameter; and

wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the revised netlist at the supplied circuit stress time values.

102.(New) The method of claim 101, wherein said simulating the behavior is performed using a circuit simulator and includes incorporating the aging of the selected components by updating the models of said circuit simulator.

103.(New) The method of claim 92, wherein said simulating the behavior is performed using a circuit simulator and includes incorporating the aging of the selected components by updating the models of said circuit simulator,

and wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit at the supplied stress time values by simulating the operation of the circuit with the each of the specified components using the respective aging model information and respective relative component degradation parameter at the supplied stress time values.

104.(New) The method of claim 92, wherein said degradation parameter is a degradation level relative to circuit stress time, the process further comprising:

quantizing each of said relative degradation levels to one of a plurality of discrete values, and

wherein said determining the degraded operation of the circuit includes determining the degraded operation of the circuit by simulating the operation of the circuit with the specified components using their respective aging model information and respective quantized relative degradation level at the supplied circuit stress time value.